## REMARKS

Claims 2-4 are pending herein. By the Office Action, claims 1-4 are rejected under 35 U.S.C. §102(b). By this Amendment, claim 1 is canceled. Support for the amendments to claims 2-4 can be found in the specification at, for example, page 10, lines 6-18 and page 11, lines 11-16. No new matter is added. Applicants respectfully request reconsideration in view of the above amendments and the following remarks.

I. Claim for Priority

The Application Transmittal filed with the application indicated that priority of foreign application No. 11-201585 filed July 15, 1999 in Japan was claimed under 35 U.S.C. §119 and/or §365(b), and that the certified copy was filed in prior Application No. PCT/JP00/04634. The present Office Action does not acknowledge the claim for priority, or confirm that the priority document was received. The Examiner is requested to confirm the claim for priority in the next Office Action.

II. §102 Rejection

Claims 1-4 are rejected under 35 U.S.C. §102(b) over Takashi (EP 0928017). Claim 1 is canceled herein, rendering the rejection of that claim moot. Applicants respectfully traverse this rejection as to claims 2-4.

A. The Invention

The claimed invention is directed to bonded wafers having a base wafer bonded to a bond wafer. The claimed bonded wafers provide significant advantages over single wafers and bonded wafers of the prior art.

According to the prior art, bonded wafers were generally produced by either (1) use of grinding and polishing processes or (2) use of hydrogen ions or rare gas ions. See specification at page 1, last paragraph and page 3, line 5 to page 4, line 9. In the first method, one of the wafers, the bond wafer, is subjected to grinding and polishing processes to reduce

its thickness to a desired thickness for subsequent fabrication of a device thereon. As a result, a SOI layer is formed on the other wafer, the base wafer. In the second conventional method, hydrogen ions or rare gas ions are implanted into a bond wafer to form a fine bubble layer. The bond wafer is then bonded to a base wafer. A portion of the bond wafer is then delaminated by using the fine bubble layer as a cleavage plane, so that a SOI layer having a very thin and uniform thickness can be provided on the base wafer.

In each of the conventional methods, a bonded wafer is formed by bonding a base wafer and a bond wafer. As such, high flatness of each bonding surface is required. Thus, conventional practice has been to use conventional wafers in which one surface, the bonding surface, is mirror polished. See specification at page 5, lines 1-5 and page 7, lines 9-13.

B. Claim 2 is Patentable Over Takashi

Claim 2 is directed to a bonded wafer having a base wafer wherein a back surface of the base wafer is chemically etched and a chamfered part of the base wafer is subjected to chamfering and mirror finishing to form a mirror surface, and on the chemically etched back surface, a maximal depth of pits is 6 μm or less and an average value of waviness is 0.04 μm or less, wherein the base wafer is bonded to a bond wafer. Such a bonded wafer is not disclosed in Takashi.

According to the invention of claim 2, if the chamfered part of the base wafer is mirror finished, and pit depth and waviness on the back surface are as stated in the claim, then generation of particles from the chamfered part and the back surface can be suppressed. Furthermore, because flatness of the back surface of the bonded wafer is extremely high, thickness uniformity of the SOI layer or silicon active layer of the bonded wafer is also extremely high. See Specification at page 16, line 10 to page 17, line 4, and page 29, Table 1 to page 30, line 4. Such bonded wafers of the claimed invention can be suitably used, for example, for fabrication of a device having a finer pattern or special structure. See

Specification at page 17, line 24 to page 18, line 15. Such a bonded wafer is not disclosed in Takashi.

Takashi is directed to semiconductor wafers. As indicated in the Office Action, Takashi discloses wafers having a maximal pit depth of 6 μm or less and an average value of waviness of 0.04 μm or less. See page 4, lines 44 and 45. Takashi discloses that the wafer can be formed by chamfering, lapping, etching, mirror polishing, and cleaning. See page 3, lines 1-4. Although Example 1 of Takashi and Example 1 of the present specification describe similar processes and wafers with similar properties, Takashi does not disclose the specific bonded wafer of the claimed invention.

In particular, the wafer of Takashi is not a bonded wafer, as claimed. The wafer of Takashi is simply one semiconductor wafer; it is not a bonded wafer having a base wafer bonded to a bond wafer, as in claim 2. Furthermore, Takashi does not disclose that the chamfered part of the semiconductor wafer is subjected to mirror finishing as in the claimed invention. Thus, the claimed wafer and the wafer of Takashi structurally differ from each other.

The Office Action argues that the process steps in claim 2 do not define the claimed product, and therefore are not given patentable weight. Applicants respectfully disagree. First, as described above and as is known in the art, the various process steps recited in claim 2 result in specific physical properties. For example, the chemical etching, chamfering, and mirror finishing referred to in the claim impart physical properties, such as the claimed maximum pit depth and maximum waviness, to the wafer surfaces. These process steps thus cannot be ignored, as they are directly linked to the structural features also recited in the claim. Furthermore, the omission of one or more of those steps in the manufacturing process of the wafer of Takashi, such as omission of the mirror finishing of the chamfered part of the semiconductor wafer, means that the structure and properties of the wafer of Takashi would

differ from the claimed invention. Thus, all of the features of claim 2 must be considered when comparing the claimed invention to Takashi.

Still further, the claimed invention differs from Takashi at least in the performance properties of the respective wafers. Inherently, a bonded wafer is superior to a common semiconductor wafer produced from a single wafer at least in terms of characteristics such as high speed of device, low electricity consumption, and the like. See specification at page 1, lines 7-15. Even if the maximum pit depth and waviness values of Takashi's wafer are comparable to those of the claimed invention, the claimed invention differs from Takashi at least because the claimed wafer is a bonded wafer, and generation of particles from the chamfered part and the back surface can be suppressed, as discussed above. The claimed bonded wafer is thus much more suitable for producing high performance devices, which have high speed, low electricity consumption, and the like.

For at least these reasons, Takashi does not anticipate the bonded wafer of claim 2. Claim 2 is thus not anticipated by Takashi.

Further, it would not have been obvious for one of ordinary skill in the art to have used the single wafer of Takashi to form a bonded wafer, as claimed. In a bonded wafer produced using two silicon wafers, a device is formed on a SOI layer. However, it would not have been obvious to one of ordinary skill in the art to have used two high quality semiconductor wafers -- one as a base wafer and one as a bond wafer -- to form a bonded wafer. The base wafer in such a structure is inherently used as a support, and the high production cost for making high quality semiconductor wafers would lead one skilled in the art away from using two such wafers, in the absence of any teachings to the contrary.

Thus, claim 2 is patentable over Takashi. Reconsideration and withdrawal of the rejection are respectfully requested.

C. Claims 3 and 4 are Patentable Over Takashi

Claim 3 is directed to a bonded wafer having a base wafer wherein a power spectrum density on a back surface of the base wafer is 0.5 to 10 $\mu m^3$ as measured by waviness having a wavelength of 10 mm, wherein the base wafer is bonded to a bond wafer. Claim 4 is directed to a bonded wafer having a base wafer wherein at least a back surface and a chamfered part of the base wafer are mirror surface and the chamfered part of the base wafer is subjected to chamfering and mirror finishing, wherein the base wafer is bonded to a bond wafer. Such bonded wafers are also not disclosed in Takashi.

Each of claims 3 and 4 specifically recite that the bonded wafer has a base wafer that is bonded to a bond wafer. However, as described in detail above, Takashi does not disclose such a bonded wafer. Takashi only discloses a single semiconductor wafer, and nowhere teaches that the wafer is bonded to a second wafer, as claimed.

For at least these reasons, Takashi does not anticipate the bonded wafers of claim 3 and 4. Claims 3 and 4 are thus not anticipated by Takashi. Reconsideration and withdrawal of the rejection are respectfully requested.

III. Conclusion

In view of the foregoing amendments and remarks, Applicants submit that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the application are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the telephone number listed below.

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Date: June 23, 2004

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